In re patent application of:
BEADLE ET AL.
Continuation of **09/391,919** filed **09/09/99**
Filed: **HEREWITH**
Serial No. **NOT YET ASSIGNED**
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In the Specification:

Please replace the first paragraph below the header CROSS-REFERENCE TO RELATED APPLICATIONS beginning at page 1, line 1, with the following rewritten paragraphs:

The present application is a continuation of U.S. Patent Application, Serial No. 09/391,919, filed September 9, 1999, by E. Beadle et al., entitled: "Dual Key Controlled Content Addressable Memory For Accessing Packet Switch Data Buffer For Multicasting Data Packets", and relates to subject matter disclosed in ~~coincidentally filed U.S. Patent Application, Serial No. /***,***~~ U.S. Patent No. 6,208,544, issued March 27, 2001, by E. Beadle et al, entitled: "Content Addressable Memory Cell Providing Simultaneous Read and Compare Capability" (hereinafter referred to as the ~~'*** application~~ '544 patent), and are assigned to the assignee of the present application and the ~~disclosure~~ disclosures of which [[is]] are incorporated herein.

Please replace the paragraph beginning on page 7, line 16, with the following rewritten paragraph.

Figure 4 corresponds to Figure 3 of the above-identified ~~'*** application~~ '544 patent, and diagrammatically illustrates the configuration of a respective content addressable bit memory

cell having simultaneous read and compare capability;

Please replace the paragraph bridging pages 17 and 18, beginning at line 19, with the following rewritten paragraph.

As noted previously, configuring the CAM 50 in the manner described in the above-referenced ~~'*** application~~ '544 patent enables the dual key and associative field searches and read operations to be performed simultaneously. This expedites reading out the contents of the N bit address association field within a buffer address pointer word for which a match of its companion K bit key field with that supplied read-out key was produced during the first CAM search. As illustrated in the flow diagram of Figure 8, this facilitates rapidly accessing that packet from the output packet buffer 30, at the same time that the CAM is being searched to determine whether the packet buffer address of interest can now be marked as free.

Please replace the paragraph bridging pages 18 and 19, beginning at line 17, with the following rewritten paragraph.

The architecture of the dual key CAM 50 is diagrammatically illustrated in Figure 2 as comprising an X by (K+N) memory cell array or matrix 70, in which the word depth X is set by the

application. The number of words X may be divided evenly into the number of queues for a given application. Alternatively, for dynamic sharing of CAM resources, the number of words X may comprise a 'pooled' resource when one queue could effectively use all the array locations, for enhanced flexibility. The matrix 70 of content addressable memory cells is preferably configured as detailed in the above-referenced ~~'*** application~~ '544 patent. Figure 3 shows the manner in which plural ones (K+N) of such memory cells are organized to form a respective dual key buffer address pointer word. The dual key buffer address pointer words, in turn, are organized into arrays of words within the memory, as shown diagrammatically in Figure 5, to be described.

Please replace the paragraph beginning on page 23, line 1, with the following rewritten paragraph.

Figure 3 shows the organization of a plurality of CAM cells as a respective dual key buffer address pointer word. For purposes of providing a non-limiting example, the illustrated dual key address pointer word is shown as being formed of a plurality of 'row'-resident bit cells. It should be observed, however, that a respective dual key buffer address pointer word may be formed of a plurality of memory cells disposed in a column of the memory cell matrix. As shown in Figure 3, the key field

portion of a buffer address pointer word contains a plurality K of key field bit cells 200-1, ..., 200-K, and a companion plurality N of association field bit cells 210-1, ..., 210-N. The configuration of a respective one of each of the key field bit memory cells 200 and association field bit memory cells 210 is diagrammatically shown in Figure 4, to be described, which corresponds to Figure 3 of the above-identified ~~'*** application~~ '544 patent.